Scientific Programme

Monday 7 Oct.

9.30-9.45 Opening address: Prof Toomas Rang
Greetings: Rector Andres Keevallik
Plenary Session

9.45-10.15 Invited talk 1
Venture Capital and Financing of Technology Projects
Olev Schults, Estonia

10.15-10.45 Invited talk 2
The European Union 6th Framework Programme for Research and Development
Javid Khan, Belgium

10.45-11.15 Invited talk 3
40 years of Electronics Department at Tallinn Technical University
Uljas Tamm, Enn Velmre, Estonia

11.15-11.30 **Coffee**

11.30-12.00 Invited talk 4
Integrated Circuit Design for Personal Communication Systems
Veikko Porra, Kari Halonen, Finland

12.00-12.30 Invited talk 5
Conceived Performance of Re-Configurable IC Architectures
Tuomas P. Valtonen, Jouni Isoaho, Hannu Tenhunen, Sweden

12.30-13.00 Invited talk 6
Processing Signals Digitally in a Much Wider Frequency Range
Ivars Bilinskis, Latvia

13.00-14.00 **Lunch**

12.00-18.00 **Tutorials on Analog and Digital Test**
TUTORIAL 1: Design for Test of Systems on Chip: Analog Test
Presenters: V. Stopjakova, V. Mosin, M. Blyzniuk

14.00-16.00 **7. Power Electronics**
⇨ Chair: J. Järvik

14.00-14.20 **New Concept of the Parallel Active Power Filtering**
Ryszard Strzelecki, Grzegorz Benysek, Jacek Rusinski, Marcin Jarnut, University of Zielona Góra, Poland

14.20-14.40 **Single phase active power line conditioners - without transformers**
G. Meckien[1], R. Strzelecki[2], [1]University of Technology& Agriculture, [2]Technical University of Zielona Gora, Poland

14.40-15.00 **Development of auxiliary power supply for tram**
D. Vinnikov, M. Lehtla, Tallinn Technical University, Estonia

15.00-15.20 **Quality factor of planar spiral inductors at frequencies up to self-resonance**
J. Jankovskis, Riga Technical University, Latvia

Monday 7 Oct.

15.20-15.40 **Power analyse of a tram system with energy storage Devices**
J. Joller, M. Lehtla, Tallinn Technical University, Estonia

15.40-16.00 **Experimental Water Treatment Systems Control and Monitoring via Multipoint Interface**
A. Rosin, T. Lehtla, Tallinn Technical University, Estonia

14.00-15.40 5. Telecommunication and Optical Transmission

⇨ Chair: A. Ots

14.00-14.20 **Detection of modulation scheme in adaptive OFDM**
A. Meister, E. Lossmann, P. Martverk, Tallinn Technical University, Estonia

14.20-14.40 **A Statistical Model for RF Wireless Channels**
A. Raja, Tallinn Technical University, Estonia

14.40-15.00 **Using fading to improve accuracy of Cell ID based mobile positioning algorithms**
Ritvars Krievs, Riga Technical University, Latvia

15.00-15.20 **A 2.4 GHz FM-DCSK Chaos Radio System**
V. Porra, K. Król*, A. Mozsàry**, Helsinki University of Technology, Finland, *presently with Spirea Inc.; **Presently with Budapest U. Tech

15.20-15.40 **Regression models CATV**
Rudolf Volner[1], Petr Boreš[2], Daša Tichá[3], [1, 3]University of Zilina, Slovak Republic, [2]CTU Prague, Czech Republic

14.00-16.00 6. Biomedical Electronics

⇨ Chair: K. Meigas

14.00-14.20 **Frequency response simulation of ultrasound contrast agent considering size distribution**
T. Burba, A. Kopustinskas, Kaunas University of Technology, Lithuania

14.20-14.40 **A survey of bioinspired methods for design of fault tolerant reconfigurable architectures**
Lukáš Sekanina, Vladimír Drábek, Brno University of Technology, Czech Republic

14.40-15-00 **A New Type of Non-Contact 2D Multimodal Interface to Track and Acquire Hand Position and Tremor Signal**
Dan-Marius Dobrea[1], Horia-Nicolai Teodorescu[1, 2], [1]"Gh. Asachi" Technical Univ. of Iasi, [2]Romanian Academy, Romania

15.00-15.20 **Electrical Bioimpedance Measurement: methods and equivalent circuits**
R. Gordon, T. Parve, Tallinn Technical University, Estonia

15.20-15.40 **A set-up for investigation of post-ischaemic recovery of isolated animal heart based on dynamic measurement of pressure, flow, and electrical bioimpedance**
I. Rätsep[1], A. Kink[1], G. Taal[2], T. Parve[2], [1]North-Estonian Regional Hospita, Estonia, [2]Tallinn Technical University, Estonia

Monday 7 Oct.

15.40-16.00 **Mean and standard deviation for ischemic stroke segmentation of human head brain in computed tomography images**
A. Usinskas, V. Mikelaitis, Vilnius Gediminas Technical University, Lithuania

16.00-16.30 **Coffee**

16.30-17.40 **Posters: 7. Power Electronics**

❒ P-006 **Two new unity power factor three-phase diode rectifiers with ripple power re-rectification and resonant filters**
T. Sakkos, V. Sarv, Tallinn Technical University, Estonia

❒ P-025 **Starting of a diesel engine by help of ultracapacitors**
V. Boiko, D. Vinnikov, J. Joller, Tallinn Technical Univ., Estonia

16.30-17.40 **Posters: 5. Telecommunication and Optical Transmission**

❒ P-003 **The evaluation of different packet size groups delay Bound**
R. Plestys, D. Rimkus, Kaunas Univ. of Technology, Lithuania

❒ P-013 **Portable optical spectrum analyzer for testing optical DWDM telecommunication systems**
T. Tõnnisson[1], J. Pelt[1], B. Vince[2], [1]Interspectrum OU, Tõravere, Estonia, [2]Spectrolab Analytical Ltd, UK

❒ P-061 **Network model ATM - based broadband CATV**
Rudolf Volne[1], Petr Boreš[2], Daša Tichá[3], [1,3]University of Zilina, Slovak Republic, [2]CTU Prague, Czech Republic

❒ P-062 **CATV - edge networks**
Rudolf Volner[1], Petr Boreš[2], Daša Tichá[3], [1,3]University of Zilina, Slovak Republic, [2]CTU Prague, Czech Republic

❒ P-078 **Long-range dependent traffic models CATV**
Rudolf Volner[1], Petr Boreš[2], Daša Tichá[3], [1,3]University of Zilina, Slovak Republic, [2]CTU Prague, Czech Republic

16.30-17.40 **Posters: 6. Biomedical Electronics**

❒ P-038 **Electronic in In Vitro Fertilisation Task**
T. Mainzer, University of West Bohemia, Czech Republic

❒ P-049 **Analog-To-Digital Conversion of Bio-Signals by Means of the PC Sound Card**
Maris Ozols and Janis Spigulis, University of Latvia, Latvia

❒ P-104 **Reduction of ocular artifacts from sleep EEG signals using the independent component analysis method**
Anca Mihaela Lazar[1], Victor Andrei Maiorescu[2], [1]UMF, Romania, [2]UTI, Romania

Tuesday 8 Oct.

9.00-10.20 **4. Test, Diagnostics, and Fault Tolerance**
Session 1. Fault tolerance and built-in test
⇨ Chair: R. Ubar

9.00-9.20 **Transient faults robustness evaluation of safety critical system using simulation**
P. Grillinger, S. Racek, Univ. of West Bohemia, Czech Republic

9.20-9.40 **Automatic Synthesis Bist Tool for Digital Circuits**
Tomáš Pikula, Mária Fischerová, Elena Gramatová, Institute of Informatics of the Slovak Academy of Sciences, Slovakia

9.40-10.00 **Low Power Boundary Scan Design**
Zdenek Plíva, Ondrej Novák, Technical University of Liberec, Czech Republic

10.00-10.20 **An experiment board for IEEE 1149.1 education**
Bengt Magnhagen, Esmail Olfati, Jonkoping University, Sweden

9.00-10.20 **2. Integrated Electronics and Chip Design**
Session 1.
⇨ Chair: V. Kukk

9.00-9.20 **A Dual-Mode 85MHz Double Sampling Bandpass $\Delta\Sigma$-Modulator**
J. Järvinen, T. Salo, K. Halonen, Helsinki University of Technology, Finland

9.20-9.40 **A CMOS Adiabatic Bus-Driver - Experimental Results**
Jacek Flak, Veikko Porra, Helsinki Univ. of Technology, Finland

9.40-10.00 **Amplifier Circuits For a 60 GHz Radio Front-End**
Mikko Kärkkäinen[1], Mikko Varonen[1], Jan Riska[1], Pekka Kangaslahti[1, 2], and Veikko Porra[1], [1]Helsinki University of Technology, Finland, [2]Ylinen Electronics, Finland

10.00-10.20 **An Integrated 2 GHz SiGe Power Amplifier**
Pasi Juurakko, Ville Saari, Jussi Ryynänen, Kari Halonen, Helsinki University of Technology, Finland

9.00-10.20 **Special Session: Digital Alias-Free Signal Processing**
⇨ Chair: I. Bilinskis room AII-208

9.00-9.20 **Analog Signal Digitizer Adapted to Experimental Evaluation of DASP Algorithms**
Ju. Artyukh, V. Bespal'ko, E. Boole, Institute of Electronics and Computer Science, Latvia

9.20-9.40 **Signal Reconstruction from Finite Sets of Arbitrarily Distributed Samples**
Andrzej Tarczynski, University of Westminster, UK

9.40-10.00 **High-resolution Event Timing Based on Analog Signal Digitizing**
Ju. Artyukh, Institute of Electronics and Computer Science, Latvia

Tuesday 8 Oct.

10.00-10.20 **A New Line of Timing Systems for Satellite Laser Ranging**
Ju. Artyukh, V. Bespal'ko, E. Boole, Institute of Electronics and Computer Science, Latvia

10.40-11.00 **Coffee**

11.00-12.20 **4. Test, Diagnostics, and Fault Tolerance Session 2. Fault simulation and diagnosis**
⇨ Chair: B. Magnhagen

11.00-11.20 **Symbolic techniques in parametric fault diagnosis of analog circuits**
F. Grasso, A. Luchetta, S. Manetti, M. C. Piccirilli, University of Florence, Italy

11.20-11.40 **Fault Diagnosis on electronical circuits based of content addressable memories**
Wolfgang Fredrich[1], Wojciech Toczek[2], [1]University of Rostock, Germany, [2]Technical University of Gdansk, Poland

11.40-12.00 **Approach to prune the list of defects by neglecting statistically insignificant shorts in standard cells defect/fault analysis**
M. Blyzniuk, I. Kazymyra, Lviv Polytechnic National University, Ukraine

12.00-12.20 **Java Technology Based Training System for Teaching Digital Design and Test**
S. Devadze[1], A. Jutman[1], A. Sudnitson[1], R. Ubar[1], H.-D. Wuttke[2], [1]Tallinn Technical University, Estonia, [2]Ilmenau Technical University, Germany

11.00-12.20 **2. Integrated Electronics and Chip Design Session 2.**
⇨ Chair: V. Männama

11.00-11.20 **Broadband Upconverter for Cable Modem Receiver**
Arto Malinen[1], Petteri Paatsila[2], Kari Stadius[1], Kari Halonen[1], [1]Helsinki University of Technology, [2]ATMEL Finland Development Center, Finland

11.20-11.40 **The non-idealities effect on the pipelined sigma-delta modulator performances**
A. Rusu, H. Tenhunen, Royal Institute of Technology (KTH), Sweden

11.40-12.00 **A Case Study on the Effects of Substrate Noise in RF CMOS Mixers**
Li Li and Hannu Tenhunen, Royal Institute of Technology (KTH), Sweden

12.00-12.20 **A 32x32 CMOS Photogate Active Pixel Sensor Matrix**
A. Leppänen[1], K. Tukkiniemi[2], [1]Prismasonic, Finland, [2]VTT Microelectronics, Finland

Tuesday 8 Oct.

11.00-12.20 **Special Session: Digital Alias-Free Signal Processing**

⇨ Chair: I. Bilinskis room AII-208

11.00-11.20 **DASP-based test system for linear circuits**

M. Greitans, Institute of Electronics and Computer Science, Latvia

11.20-11.40 **DASP-based processing of telecommunication signals**

I. Mednieks, Institute of Electronics and Computer Science, Latvia

11.40-12.00 **Scalable VHDL Architectures for Non-Uniform Sampling Driver Designs**

F. Papenfuß, R. Hecht, D. Timmermann, University of Rostock, Germany

12.00-12.20 **Pseudorandom Sampling in a Multi-frequency Bioimpedance Analyser**

O. Märtens[1], M. Min[1,2], [1]Tallinn Technical University, Estonia, [2]Cybernetica AS, Estonia

12.40-14.00 **Lunch**

14.00-15.20 **4. Test, Diagnostics, and Fault Tolerance Session**
3. Test pattern generation

⇨ Chair: E. Gramatova

14.00-14.20 **High-Level Synthesis and Test in the MOSCITO-Based Virtual Laboratory**

A. Schneider[1], K.-H. Diener[1], G. Jervan[2], Z. Peng[2], J. Raik[3], R. Ubar[3], T. Hollstein[4], M. Glesner[4], [1]Fraunhofer Institute for Integrated Circuits (IIS/EAS), Germany, [2]Linköping University, Sweden, [3]Tallinn Technical University, Estonia, [4]Technical University of Darmstadt, Germany

14.20-14.40 **Genetic algorithms in test generation for digital circuits**

Y.A. Skobtsov[1], D.E. Ivanov[2], V.Y. Skobtsov[2], S.A. Zakusilo[2], [1]DNTU, Ukraine, [2]Institute of Applied Mathematics and Mechanics Of NAS of Ukraine, Ukraine

14.40-15.00 **Automatic Test Patterns Generation for Simulation-based Validation**

V. Jusas, R. Šeinauskas, Kaunas University of Techology, Lithuania

15.00-15.20 **ATPG System and Test Genaration Methods for Digital Devices**

Vladimir Hahanov, Olga Skvortsova, Irina Sysenko, Hayk Chamyan, Kharkov National University of RadioElectronics, Ukraine

Tuesday 8 Oct.

14.00-15.00 **2. Integrated Electronics and Chip Design Session 3.**

⇨ Chair: E. Kängsep

14.00-14.20 **Using Weighted Graphs for Fast Architecture Exploration**

Peeter Ellervee, Tarmo Klaar*, Margus Kruus, Kalle Tammemäe, Tallinn Technical University, Estonia, *MicroLink Computer Ltd., Estonia

14.20-14.40 **Artificial Neural Network in analog VLSI-Technology**

Gundolf Geske[1], Frank Stüpmann[2], Steffen Rode[3], [1]University of Rostock, [2,3]Neurosystems, Germany

14.40-15.00 **SC Structures with Low-Threshold MOS Switches**

V. Männama and R. Sabolotny, Tallinn Technical Univ., Estonia

15.40-16.00 **Coffee**

Tuesday 8 Oct.

16.00-17.40 **Posters:**
4. Test, Diagnostics, and Fault Tolerance

❒ P-073 **Defect-Oriented Test Generation and Fault Simulation in the Environment of MOSCITO**
A. Schneider[1], K.-H. Diener[1], E. Gramatova[2], M. Fisherova[2], E. Ivask[3], R. Ubar[3], W. Pleskacz[4], W. Kuzmicz[4], [1]Fraunhofer Institute for Integrated Circuits (IIS/EAS), Germany, [2]Institute of Informatics, Slovak Republic, [3]Tallinn Technical University, Estonia, [4]Warsaw University of Technology, Poland

❒ P-042 **Aspects of Complex Electronic Systems Reliability**
P. Balaišis, D. Eidukas, D. Navikas, A. Besakirskas, Kaunas University of Technology, Lithuania

❒ P-079 **Parallel Fault Simulation in Functional-Switching CMOS-Structures**
A. E. Lyulkin, I. I. Linnik, Belarussian State University, Belarus

❒ P-077 **A Novel 1-out-of-n differential CMOS checker and its Applications to Fault Tolerant Designs**
Jimson Mathew, Elena Dubrova, Royal Institute of Technology (KTH), Sweden

❒ P-086 **Exact Static Compaction of Independent Test Sequences**
J. Raik, A. Jutman, R. Ubar, Tallinn Technical University, Estonia

16.00-17.40 **Posters:**
2. Integrated Electronics and Chip Design

❒ P-035 **High Speed Learning in Silicon**
F. Stüpmann, S. Rode, G. Geske, NEUROSYSTEMS GmbH, Germany

❒ P-040 **Models of SAW Sensors**
S. Rupkus, Kaunas University of Technology, Lithuania

❒ P-043 **Research of Electronic Devices Thermal States Dynamics**
P. Balaišis, D. Eidukas, D. Navikas, G. Vilutis, Kaunas University of Technology, Lithuania

❒ P-102 **An approach to accuracy improvement of the noise macromodels in the general-purpose circuit simulators**
E. Gadjeva, M. Hristov, B. Mihova, L. Donevska, Technical University of Sofia, Bulgaria

❒ P-105 **Survivable synchronous sequential circuits design**
A. Matrosova, V. Andreeva, Tomsk State University, Russia

Wednesday 9 Oct.

9.00-18.00 **Tutorials on Analog and Digital Test**
TUTORIAL 2: Design for Test of Systems on Chip: Digital Test
Presenters: J. Hlavicka, V. Drabek, O. Novak, Z. Pliva, Z. Kotasek, E. Gramatova

9.00-10.20 **1. Electronic Materials, Devices, and Simulation**
8. Micromechanical Systems
Session 1.
⇨ Chair: A. Udal

9.00-9.20 **Design and Prototyping of Embedded Systems-on-Chip for Mechatronic Systems**
T. Hollstein, R. Ludewig, C. Schlachta, M. Glesner, Darmstadt University of Technology, Germany

9.20-9.40 **Interface Circuit for a Micromechanical Microphone Read-out**
Jouko Marjonen[1], Arto Rantala[1], Markku Åberg[1], Hannu Sipola[2], [1]VTT Electronics, [2]VTT Automation, Finland

9.40-10.00 **Simulation of the Twined Helical Deflecting System**
S. Štaras, T. Burokas, Vilnius Gediminas Technical University Lithuania

10.00-10.20 **Wireless Internet Equipment Security Modelling**
D. Eidukas, A. Valinevicius, M. Silys, Š. Kilius, Kaunas University of Technology, Lithuania

9.00-10.20 **3. Instrumentation and System Design**
Session 1.
⇨ Chair: M. Min

9.00-9.20 **Application of content addressable memories for the design of PCB**
Wolfgang Fredrich, University of Rostock, Germany

9.20-9.40 **Transparency Enhancement of First Order Takagi-Sugeno Systems: Promoting the Competition Between the Rules by Controlling the Overlap of Input Fuzzy Sets**
Andri Riid, Raul Isotamm, and Ennu Rüstern, Tallinn Technical University, Estonia

9.40-10.00 **Fuzzy Hierarchical Control of Truck and Trailer**
Andri Riid and Ennu Rüstern, Tallinn Technical University, Estonia

10.00-10.20 **Coherence function and Wiener-Hammertein systems**
Tadeusz P. Dobrowiecki, Johan Schoukens, Budapest University of Technology and Economics, Hungary

10.40-11.00 **Coffee**

Wednesday 9 Oct.

11.00-12.20 **1. Electronic Materials, Devices, and Simulation**
8. Micromechanical Systems
Session 2.
⇨ Chair: E. Velmre

11.00-11.20 **Two-dimensional nonisothermal analysis of the current crowding effect at nonuniform SiC Schottky contacts using device simulator DYNAMIT-2DT**
Raido Kurel, Andres Udal, Tallinn Technical University, Estonia

11.20-11.40 **Preliminary Investigation of Diffusion Welded Contacts to p-type 6H-SiC**
O. Korolkov, T. Rang, N. Kuznetsova, and J. Ruut, Tallinn Technical University, Estonia

11.40-12.00 **Modelling of the Seebeck coefficient influenced by carrier phonon drag and mixed scattering**
M. Milatškov, Tallinn Technical University, Estonia

12.00-12.20 **Classical Electrodynamics, Charge Distributions of Currents and the Metal Transistor**
Rainer Taniloo, Tallinn Technical University, Estonia

11.00-12.20 **3. Instrumentation and System Design**
Session 2.
⇨ Chair: T. P. Dobrowiecki

11.00-11.20 **Frequency pattern fitting in an extended block-adaptive Fourier analyser - I: indipensable restrictions**
Ants Ronk, Tallinn Technical University, Estonia

11.20-11.40 **Linear Interpolation of Nonlinear Functions with Minimized Number of Knots for DSP Applications**
Peteris Misans[1], Normunds Veselis[2], Janis Martinsons[2], Maris Alberts[2], [1]Riga Technical University, Latvia, [2]University of Latvia, Latvia

11.40-12.00 **Use of multichannel sonar A1-P0-PCI in bathymetric surveys**
M. Rüütel[1] , V. Kozevnikov[2], P. Väling[3], [1]OÜ R-Süsteemid, [2]Tallinn Technical Univ., [3]Estonian National Maritime Board, Estonia

12.00-12.20 **Web-based Tools for Finite State Machine Decomposition with Analysis of Information Flows**
E. Fomina, A. Keevallik, M. Kruus, and A. Sudnitson, Tallinn Technical University, Estonia

12.00-12.20 **A pen for automatic signature authentication**
V. Vavricka, K. Dudacek, Uni. of West Bohemia, Czech Republic

12.40-14.00 **Lunch**

Wednesday 9 Oct.

14.00-15.40 **3. Instrumentation and System Design**
Session 3.
⇨ Chair: P. Misans

14.00-14.20 **Phase-Domain Modeling of the PLL Frequency Synthesizers**
Toivo Paavle, Tallinn Technical University, Estonia

14.20-14.40 **Realisation & application of a transconductance feedback amplifier**
M. Al-Gahtani & B. Wilson, University of Manchester Institute of Science & Technology (UMIST), UK

14.40-15.00 **Automatic Vessel Identification System**
R. Haavel, H. Tani, Department Navigation Systems of Cybernetica AS, Estonia

15.00-15.20 **Design of Digital Fluxgate Magnetometer**
A. Cerman, P. Ripka, Czech Technical University, Czech Republic

15.20-15.40 **Low Distortion Sine Wave Generator Measurements and Lock-In Amplifier**
D. Varga, J. Roztocil, Czech Technical University in Prague, Czech Republic

14.00-15.40 **Posters:**
1. Electronic Materials, Devices, and Simulation
8. Micromechanical Systems

❒ P-041 **Quality Problems of Colour Television Tubes**
R. Anilionis, G. Kondrotas, Kaunas University of Technology, Lithuania

❒ P-059 **A hybrid method for ray tracing simulation**
Juris Ziemelis, Riga Technical University, Latvia

❒ P-066 **The Structure of FET-Based Negative Differential Resistance for Microwave and Neural Network Applications**
Rainer Taniloo, Tallinn Technical University, Estonia

❒ P-089 **Simulation of the Control System of AC Linear Positioning Drive**
L. Liivik, R. Jansikene, Tallinn Technical University, Estonia

❒ P-113 **Design Sensitivity Analysis of an Angular Rate Sensor**
Saulius Kaušinis, Rimantas Barauskas, Kaunas University of Technology, Lithuania

15.40-16.00 **Coffee**

Wednesday 9 Oct.

16.00-17.40 **Posters:**
3. Instrumentation and System Design

❒ P-014 **Formation and processing of the orthogonal sounding signals in multichannel sonars**
A. Duhnik , V. Kozevnikov, Tallinn Technical University, Estonia

❒ P-015 **Sonar Adaptation to the Measurement Range**
J. Derkach, V. Kozhevnikov, Tallinn Technical University, Estonia

❒ P-046 **Measurement of the Root-Mean-Square Value of Periodic Signals on the Basis of Frequency Measurement**
A. Citavicius, V. Knyva, Kaunas University of Technology, Lithuania

❒ P-047 **Model of CRT Deflection Systems Magnetic Shunts**
O. Zimarinas, Kaunas University of Technology, Lithuania

❒ P-055 **Control and Remote Monitoring System of Aids to Navigation**
R. Haavel[1], Ü. Heinla[2], L. Käärmann[3], T. Pikpoom[4], R. Rebane[5], H. Tani[6], [1,2,4,5,6]Department Navigation Systems of Cybernetica AS, [3]Estonian National Maritime Board, Estonia

❒ P-056 **Behavioural descriptions of electronic devices and its implementation in VHDL-AMS**
M.A. Trofimov, S.G. Mosin, V.N. Lantsov, Vladimir State University, Russia

❒ P-076 **Practical measurements on new types of magnetoresistive sensors**
M. Vopálenský[1], P. Ripka[1], M. Tondra[2], H. Hauser[3], [1]Czech Technical University, Czech Republic, [2]NVE Corporation, USA, [3]Vienna University of Technology, Austria

❒ P-085 **Frequency pattern fitting in an extended block-adaptive Fourier analyser - II: ordering of frequencies and fitting of them on disjoint sets of values**
Ants Ronk, Tallinn Technical University, Estonia

❒ P-108 **Frequency pattern fitting in an extended block-adaptive Fourier analyser - III: necessary detunings**
Ants Ronk, Tallinn Technical University, Estonia

❒ P-112 **Linear Interpolation of Nonlinear Functions with Minimized Number of Knots for Fixed-Point DSP Applications**
Peteris Misans[1], Normunds Veselis[1], Janis Bleiers[2], Gints Linis[2], [1]Riga Technical University, Latvia, [2]University of Latvia, Latvia

❒ P-115 **Universal ADC testing software**
J. Brossmann, D. Varga, J. Roztocil, CTU FEE Prague, Czech Republic

Tutorials on Analog and Digital Test

Monday, October 7, 2002. 12:00 am - 6:00 pm

TUTORIAL 1: Design for Test of Systems on Chip: Analog Test

Presenters: V. Stopjakova , V.Mosin, M.Blyzniuk

The tutorial is focused on the overview of on-chip test strategies for complex mixed-signal systems, methods of testing analog circuits, and methods of defect analysis in VLSI circuits. The advanced trends in recent VLSI circuits production lead towards extremely complex systems on chip that include both digital and analog parts, and memory architectures. Testing has to keep pace with circuits design development to provide the required quality of production. Adaptive multi-parametric test methods able to handle defect detection in SoC realised in deep sub-micron technologies might be a solution. The place of testing in the life-cycle of electronic devices, complexity and cost issues, the features of faults in analog circuits, testability of analog circuits, testing and fault diagnosis, functional and structural testing, hierarchical test approaches, built-in self-test in analog circuits, methodology for probabilistic modelling of physical defects in CMOS gates and estimation of the effectiveness of test patterns for detecting physical defects will be discussed.

Wednesday, October 9, 2002. 9:00 am - 6:00 pm

TUTORIAL 2: Design for Test of Systems on Chip: Digital Test

Presenters: J.Hlavicka, V.Drabek, O.Novak, Z.Pliva, Z.Kotasek, E.Gramatova

The tutorial is focused on diagnostic methods and design for testability of integrated circuits. An overview of nowadays design for testability tools and the problems of testability will be presented. A classification and short description of bioinspired methods (phylogenetic, ontogenetic and epigenetic principles) applied for design of fault tolerant reconfigurable systems in recent years will be discussed. Different methods of built-in self-test methods and a short overview of the theory of partial scan for built-in test will be given. Low efficiency of the classical stuck at fault model in real defect coverage in MOS logic has initiated the need of new test approaches. Defect classification, taxonomy of fault models, and advanced test pattern generation algorithms will be presented as a perspective basis for achieving high defect coverage in digital circuits. The tutorials are organized in the frame of the EC Project REASON.

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